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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,164	08/25/2000	Yih-Feng Chyan	15-6-9	6246

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EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,164	CHYAN ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *20-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-19* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. A question has arisen as to the precise publication date of the following:

Hergenrother, J.M., ET AL., "The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET With Lithography-Independent Gate Length", I.E.E.E., 4 pages (Mar., 1999).

Reinberg (6,300,199) cites this paper and asserts it was published in March 1999. Other sources, possibly citing reprints, report September, November, and December 1999 as the publication date. Two of the current applicants appear to have contributed to this paper, and they are asked to supply its precise publication date.

Election/Restriction

2. Applicant's election with traverse of Group I claims 1-19 in Paper No. 6 is acknowledged. The traversal is on the ground(s) that the method claims of Group II are patentably distinct over the product claims of Group I, and that if the limitation "formed along a plane" in claim 1 is read broadly enough to include "formed in a trench" or "formed on a rounded surface," then the method of Group II can make no device that is materially different from the device claimed in Group I. This is not found persuasive because a product formed in a trench is considered to be materially different from the claimed product, formed along a plane, and the inventions are distinct if the process as

claimed can be used to make other and materially different product. See (MPEP § 806.05(f)).

The requirement is still deemed proper and is therefore made FINAL.

Oath/Declaration

3. The oath/declaration filed on 01/29/01 is acceptable.

Drawings

4. The drawings are objected to by the PTO Draftsperson for the reasons noted on the attached Notice of Draftsperson's Patent Drawing Review, form PTO-948. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Color photographs and color drawings are acceptable only for examination purposes unless a petition filed under 37 CFR 1.84(a)(2) is granted permitting their use as acceptable drawings. In the event that applicant wishes to use the drawings currently on file as acceptable drawings, a petition must be filed for acceptance of the color photographs or color drawings as acceptable drawings. Any such petition must be accompanied by the appropriate fee set forth in 37 CFR 1.17(h), three sets of color drawings or color photographs, as appropriate, and an amendment to the first paragraph of the brief description of the drawings section of the specification which states:

The patent or application file contains at least one drawing executed in color. Copies of this patent or patent application publication with color drawing(s) will be provided by the U.S. Patent and Trademark Office upon request and payment of the necessary fee.

Color photographs will be accepted if the conditions for accepting color drawings have been satisfied.

Priority

5. Applicants have made no claim for priority.

Information Disclosure Statement

6. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

If applicants are aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Specification

7. Applicants are reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 250 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

8. The abstract of the disclosure is objected to because:

A. The abstract exceeds 250 words in length.

B. The abstract does not concisely point out the invention claimed.

C. The abstract is not clearly indicative of the invention to which the claims are directed.

Correction is required. See MPEP § 608.01(b).

9. The disclosure is objected to because of the following informalities:

A. On page 3 line 20 Applicants refer to "U.S. Serial number 290533." This reference misidentifies application number 09/335,646 filed 6/18/99, and must be corrected.

B. On page 3 line 26 Applicants refer to "U.S. Serial number 341,190." This reference misidentifies application number 09/528,753 filed 03/20/2000, and must be corrected.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "the diffusion regions" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Correction is required.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-13, 15,16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over FITCH ET AL. (5,414,289) in view of WOO ET AL. (5,408130).

With regard to claims 1-13, Fitch ET AL. discloses an integrated circuit structure 11 comprising a semiconductor layer 40-42 having a major surface formed along a plane, first 44 and second 46 spaced-apart doped regions formed in the surface, wherein the first and second doped regions are first and second source/drain regions, a third doped region 50, being a first channel region, over the first region of different conductivity type than the first region, an electrical connection between the doped regions, a fourth doped region 58, being a second channel region, over the second region, of different conductivity type than the second region, a fifth doped region 60 over the fourth doped region of the same conductivity type as the second region, a sixth doped region 52 over the third doped region of the same conductivity type as the first region, the fifth and sixth doped regions being third and fourth spaced-apart source/drain regions, said first, second, third, fourth, fifth and sixth regions and conductive layer configured as two interconnected transistors of complementary conductivity type, one being a MOSFET, the transistors being configured to form an inverter circuit, further comprising a conductive element 18 connected to simultaneously control operation of both transistors wherein the conductive element comprises polysilicon and the transistors each include a gate contact region 22 adjacent the channel region and connected to the conductive element, said transistors configured to form an inverter circuit function. Note figure 9 of Fitch ET AL. Fitch ET AL. discloses a silicide interconnection between doped regions 44

and 46, see column 7 lines 37-39, but so far as specifics go Fitch ET AL. does not disclose a conductive layer comprising one or more materials taken from the group tungsten silicide, tungsten nitride, titanium silicide, titanium nitride and cobalt silicide formed between the first and second regions and above the plane to provide the electrical connection between the doped regions, wherein the conductive layer is a continuous film extending from the first region to the second region.

However, Woo ET AL. discloses an integrated circuit structure 19 with an interconnect made from a conductive layer 15 comprising tungsten or titanium silicide. Note figure 3 and column 3 lines 51-60 of Woo ET AL. Therefore, it would have been obvious to a person having skill in the art to make manifest the metal silicide interconnection suggested by Fitch ET AL. for the semiconductor device 11 with the conductive layer such as taught by Woo ET AL. in order to provide the interconnection disclosed as being needed by Fitch ET AL. but not supplied in detail by the Fitch ET AL reference.

With regard to claims 15,16, and 19 Fitch ET AL. discloses a semiconductor device 11 comprising a first layer 10 of semiconductor material, a first field effect transistor having a first source/drain region 44 formed in the first layer, a channel region 50 formed over the first layer and a second source/drain region 52 formed over the channel region, a second field effect transistor having a first source/drain region 46 formed in the first layer, a channel region 58 formed over the first layer and a second source/drain region 60 formed over the channel region; and the first and second transistors are connected to form a circuit. Note figure 9 of Fitch ET AL. Fitch ET AL. teaches an interconnection be-

tween the first source/drain regions of the first and second transistors and suggests that the connection might metal, poly, or poly/metal silicide, but does not specifically disclose a conductive layer comprising a metal positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region, wherein the conductive layer comprises a metal silicide.

However, Woo ET AL. discloses a semiconductor device with a conductive layer 15 comprising a metal, being part of a silicide such as tungsten or titanium silicide, overlying a planar surface of a layer 10, positioned between active elements such as the transistors of claims 15,16, and 19. Note figure 3 of Woo ET AL. Therefore, it would have been obvious to a person having skill in the art to make manifest the metal silicide interconnection suggested by Fitch ET AL. for the semiconductor device 11 with the conductive layer such as taught by Woo ET AL. in order to provide the interconnection disclosed as being needed by Fitch ET AL. but not supplied in detail by that reference.

B. Claim 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over FITCH ET AL. (5,414,289) in view of WOO ET AL. (5,408130), as applied to claim 15 above, and further in view of BATRA ET AL. (5,744846).

FITCH ET AL. and WOO ET AL. disclose all the limitations of claim 18 except plurality of additional field effect transistors each having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region, the first, second and additional transistors configured into a circuit wherein four of the additional transistors are connected with the first and

second transistors to form an SRAM circuit cell. Note figure 9 of Fitch ET AL.and figure 3 of Woo ET AL.

However, Batra ET AL. discloses connecting 4 additional transistors to 1st and 2nd transistors to form an SRAM circuit. Note figure 1 of Batra ET AL. Therefore, it would have been obvious to a person having skill in the art to connect 4 additional transistors, all with the limitations of the first and second transistors of claim 15, to the 1st and 2nd transistors of claim 17 to form an SRAM circuit, such as taught by Batra ET AL. in order to supply a compact memory device having 6 identically manufactured transistors thus saving manufacturing steps.

Allowable Subject Matter

12. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Papers related to this application may be submitted to Technology Center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 3-C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The

Group 2826 Fax Center number is (703) 308-7722 and 308-7724. The Group 2800 Fax Center is to be used only for papers related to Group 2800 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to Thomas Dickey whose telephone number is **(703) 308-0980**. The Examiner is in the Office generally between the hours of 8:00 AM to 5:00 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**.

TLD
03/2002

Minh Loan Tran
Primary Examiner